REMARKS

The courtesy of Examiner Huisman in granting the interview of September 7, 2005, and the helpful comments proffered at that time are acknowledged with appreciation. This response amends Claims 1, 14 and 16 to ensure allowance of Claims 1-19. Now pending in the application are Claims 1-19, of which Claims 1, 14 and 16 are independent. Support for the amendments appear in the specification on page 6, line 14-16; page 7, line 26; Figure 6 and 11; and throughout the specification. The amendments present no new matter and they present no new issues. Thus, consideration of the proposed amendments requires no further search.

Claim Rejections under 35 U.S.C. §102

Claims 1-19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,631,452 of Lin (hereinafter "Lin"). Applicants respectfully traverse each of these rejections for reasons discussed below. For ease of the discussion below, each respective related claim set is discussed separately.

Rejection of Claims 1-13 under 35 U.S.C. §102:

Claims 1-13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments.

Amended independent Claim 1 recites a microprocessor that includes a detector for detecting an imminent register window overflow or underflow condition. The microprocessor also includes an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap to *avoid* stalling the microprocessor. The trap performs at least one of a register window spill operation or a register window fill operation responsive to the condition that is detected as imminent.

Applicants respectfully submit that Lin fails to disclose each and every element of amended Claim 1. More specifically, Applicants submit that Lin fails to disclose that the microprocessor avoids a trap performing at least one of the register window spill operation or a register window fill operation to *avoid* stalling the microprocessor.

Claims 2-13 depend directly or indirectly upon amended Claim 1, and therefore, incorporate the patentable features of amended Claim 1.

Lin discloses an architecture for mandatory and speculative spill/fill operations. According to Lin, the mandatory spill/fill operations (MOP) is performed when RSE related instructions (RI) are monitored and registers are not available in the register stack. *See*, column 8, lines 58-65 of Lin. More specifically, mandatory spill/fill operations may cause the processor to stall if the active procedure cannot make forward progress until the mandatory spill/fill operations are complete. *See*, column 3, lines 2-5 of Lin.

Lin further discloses a speculative spill/fill operation, which in the words of Lin are opportunistic spill/fill operations performed when RI is not monitored and bandwidth is available. More specifically, Lin requires three conditions to be met before opportunistic spill/fill operations are performed, otherwise a mandatory spill/fill operation will occur if necessary. The three conditions required for a speculative or opportunistic spill/fill operation include an empty instruction slot must be identified in a load/store unit of the processor, a predetermined level of processor bandwidth must be available, and the mode in which the RSE operates must allow for speculative spill/fill operations. Thus, depending on the mode of operation for the RSE, the available processor bandwidth, and the availability of empty instructions slot in a load/store unit the processor architecture disclosed by Lin performs speculative spill/fill operations to reduce, not avoid, the need for mandatory spill and fill operations. *See*, column 2, line 66 to column 3, line 5.

In contrast to Lin, a microprocessor in accordance with Claim 1 includes, amongst other features, a detector detecting that one of a register window overflow condition or a register window under flow condition is imminent and an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to *avoid* a trap to *avoid* stalling the microprocessor. That is, Lin performs an opportunistic spill/fill operation exclusively when an empty instruction slot is identified in a load/store unit of the processor, sufficient bandwidth in the processor is available and upon detection of RI instructions. Thus, even if an instruction in the load/store unit of the processor indicates a spill or fill operation is likely to occur the architecture taught by Lin cannot avoid a trap and cannot avoid stalling the microprocessor unless all conditions required for a speculative spill/fill operation are met. Moreover, given the conditions required to perform a speculative spill/fill operation according to Lin, processor states or data states that indicate one of a register

overflow condition and a register window underflow condition is imminent or ready to take place are not accounted for. Furthermore, the speculative spill and fill operation of Lin merely reduce the need for mandatory spill and fill operation and since mandatory spill and fill operations may cause the processor to stall, Lin does not *avoid* stalling the microprocessor and hence does not disclose a detector and an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap to *avoid* stalling the microprocessor. Thus, Lin does not anticipate amended Claim 1.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 1-13 under 35 U.S.C. §102(e).

Rejection of Claims 14-15 under 35 U.S.C. §102:

Claims 14 and 15 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments.

Claim 15 depends from amended independent Claim 14, and therefore, incorporates the patentable features of amended Claim 14.

Amended independent Claim 14 recites a microprocessor that includes a detector for detecting an instruction in a cache prior to execution of the instruction that indicates a trap requiring an access to storage to manage register window information is imminent.

Applicants respectfully submit that Lin fails to disclose each and every element of the claimed invention. More specifically, Applicants submit that Lin fails to disclose a microprocessor that includes a detector for detecting an instruction in a cache prior to execution of the instruction that indicates a trap requiring an access to storage to manage register window information is imminent and an instruction generator responsive to the detector for generating at least one instruction to avoid the trap. The trap performing at least one of a register window spill operation or a register window fill operation.

Lin discloses mandatory and speculative spill/fill operations. In Figure 6 of the Lin reference, the mandatory spill/fill operation (MOP) is performed when RSE related instructions (RI) are monitored and registers are not available in the register stack. *See*, Lin, column 8, lines 58-65. The speculative, or in the words of Lin, opportunistic spill/fill operation is performed when RI is not monitored, sufficient bandwidth (BW) is available and an empty instruction slot is identified. In the mandatory spill/fill operation, if necessary, the

processor is stalled until the mandatory spill/fill operation is completed. *See*, Lin, column 3, line 2-5. Lin discloses that the mandatory spill/fill operations are not avoided but merely reduced by the opportunistic spill/fill operations.

Moreover, Lin does not disclose the processor includes a detector for detecting an instruction in a cache prior to execution of the instruction indicating that a trap requiring an access to the storage to manage register window information is imminent. Lin avoids a mandatory spill/fill operation if bus bandwidth is available without regard for what instructions are in cache. That is, Lin requires an empty instruction slot to perform speculative spill/fill operations and therefore monitors for the absence of an instruction, not for an instruction indicating a trap.

In the Office Action, it is noted that Lin teaches instructions are stored in an instruction cache and they are fetched from the instruction cache to be decoded and eventually executed. However, in contrast to Claim 14, Lin monitors instructions to carry out a mandatory spill/fill operation. That is, the microprocessor of Claim 14 detects an instruction in a cache prior to execution of the instruction that indicates a trap requiring an access to storage to manage register window information is imminent. For at least these reasons, Applicants contend Lin does not anticipate amended Claim 14.

Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claim 14 under 35 U.S.C. §102(e).

Rejection of Claims 16-19 under 35 U.S.C. §102:

Claims 16-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments. Amended independent Claim 16 recites a method performed in a microprocessor having a plurality of registers logically partitioned into register windows and a storage for storing contents of register windows. Performance of the method in the microprocessor determines that one of a register window overflow condition and a register window underflow condition is imminent by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache. Applicants respectfully submit that Lin fails to disclose each and every element recited in amended Claim 16.

Claims 17-19 depend directly or indirectly upon amended independent Claim 16, and therefore, incorporate the patentable features of amended Claim 16.

As discussed above in relation to the rejections of Claims 1-15, Lin discloses mandatory and speculative or opportunistic spill/fill operations. Lin monitors instructions to identify the mandatory spill/fill operations, monitors for, amongst other conditions, an empty instruction slot to perform the opportunistic spill/fill operations. However, Lin does not perform a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache to determine that one of a register window overflow condition and a register window underflow condition is imminent.

Lin monitors a load/store unit of the processor for empty instruction slots and injects speculative load/store operartions for the register file when available instructions slots are identified. That is, Lin does not perform a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache to determine that one of the register window overflow condition and a register underflow condition is imminent. In fact, Lin requires an empty instruction slot and therefore cannot perform a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache since no instruction exists.

Amended Claim 16 includes the step of determining that one of a register window overflow condition and a register window underflow condition is imminent by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache. Nowhere does Lin disclose such a step. For at least these reasons, Lin fails to anticipate Claims 16-19.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 16-19 under 35 U.S.C. § 102(e).

CONCLUSION

In view of the remarks set forth above, applicants contend that s 1-19, presently pending in the application, are patentable and in condition for allowance. If the Examiner deems that there are any remaining issues, we invite the Examiner to call the undersigned at 617-227-7400.

Respectfully submitted,
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